AMENDMENTS TO THE SPECIFICATION

Please replace the second full paragraph on page 7 of the Specification (paragraph 0018 in the patent application publication) with the following paragraph:

Rather than employing a single monolithic cache, cache-coherent CPU device 200 physically partitions the caching resources into smaller, more implementable portions. Caches 210, 215 and 220 are distributed across all ports (e.g., 261, 262, and 263) on the device, such that each cache is associated with an I/O component. According to an embodiment of the present invention, cache 210 is physically located on the device nearby I/O component 230 being serviced. Similarly, cache 215 is located proximately to I/O component 235 and cache 220 is located proximately to I/O component 240, thereby reducing the latency of transaction data requests. This approach minimizes the latency for "cache hits" and performance is increased. This arrangement is particularly useful for data that is prefetched by I/O components 230, 235 and 240.